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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/677,791	10/02/2003	Isao yamamoto	PRM-0002	9575

7590 01/26/2007

CANTOR COLBURN LLP
55 Griffin Road South
Bloomfield, CT 06002

EXAMINER	
RUTLAND WALLIS, MICHAEL	
ART UNIT	**PAPER NUMBER**
2836	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	**Application No.** 10/677,791	**Applicant(s)** YAMAMOTO ET AL.
	Examiner Michael Rutland-Wallis	**Art Unit** 2836

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 November 2006*.
2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4 and 6-10* is/are pending in the application.
4a) Of the above claim(s) *6-10* is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☐ Claim(s) *1,2 and 4* is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☒ The drawing(s) filed on *02 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a)☒ All b)☐ Some * c)☐ None of:
1.☒ Certified copies of the priority documents have been received.
2.☐ Certified copies of the priority documents have been received in Application No. _____.
3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date *11/22/2006*.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1, 2 and 4 have been considered but are moot in view of the new grounds of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takano Yoichi (JP Pub No. 2001-274332) (hereinafter "Yoichi") in view of (JP 49-135151) hereinafter referred to "Citation 2"

With respect to claim 1 Yoichi teaches a semiconductor device, including: an IC chip including: a control circuit (item 22) which, based on an input signal and a feedback signal in which an output voltage is fed back, controls the output voltage; an output pad (item 28) for outputting the output voltage; and a feedback pad (item 36) for inputting the feedback signal. Yoichi does not teach the use of a protective resistor connected between the output pad and the feedback pad. Citation 2 teaches a semiconductor device, which has output pads 1a-1c and second pad(s) 1d, where bonding wire failure is detected, based on a change in resistance between the pads, see connection of resistors R1-R3. Citation 2 teaches (see Fig. 2) connecting the voltage divider wherein the resistor among the output voltage detection terminals in the direct-current regulated power supply (item 7), and preventing the resistor of dividing voltage 11 (which is equivalent to protective resistor) from generating the abnormal voltage in circuit of voltage feedback for breaking between the detector terminal 4 and the load 2. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Yoichi to include the protective resistor between the output pad and feedback pad in order to detect and/or prevent an abnormal voltage generated by breaking the wire between the detector terminal and the load.

With respect to claim 2 Yoichi teaches a semiconductor device, including: an IC chip including: a control circuit (item 22) which, based on an input signal and a feedback signal in which an output voltage is fed back, controls the output voltage; and an output pad (item 28) for outputting the output voltage; and a feedback pad (item 36) for inputting the feedback signal; an output terminal (item 32) connected to the output pad; and a feedback terminal (item 44) connected to the feedback pad. Yoichi does not teach the use of a protective resistor connected between the output pad and the feedback pad. Citation 2 teaches (see Fig. 2) connecting the voltage divider wherein the resistor among the output voltage detection terminals in the direct-current regulated power supply (item 7), and preventing the resistor of dividing voltage 11 (which is equivalent to protective resistor) from generating the abnormal voltage in circuit of voltage feedback for breaking between the detector terminal 4 and the load 2. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Yoichi to include the protective resistor between the output pad and feedback pad in order to detect and/or prevent an abnormal voltage generated by breaking the wire between the detector terminal and the load.

With respect to claim 4 Yoichi teaches a semiconductor device, including: an IC chip including: a control circuit (item 22) which, based on an input signal and a feedback signal in which an output voltage is fed back, controls the output voltage; and an output pad (item 28) for outputting the output voltage; and a feedback pad (item 36) for inputting the feedback signal; an output terminal (item 32) connected to the output pad; and a feedback terminal (item 44) connected to the feedback pad. Yoichi does not teach the use of a protective resistor connected between the output pad and the feedback pad. Citation 2 teaches (see Fig. 2) connecting the voltage divider wherein the resistor among the output voltage detection terminals in the direct-current regulated power supply (item 7), and preventing the resistor of dividing voltage 11 (which is equivalent to protective resistor) from generating the abnormal voltage in circuit of voltage feedback for breaking between the detector terminal 4 and the load 2. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Yoichi to include the protective resistor between the output pad and feedback pad in order to detect and/or prevent an abnormal voltage generated by breaking the wire between the detector terminal and the load. Citation 2 also teaches an output interconnection which connects the output terminal (such as terminal 3) with the input terminal (connected to control item 9) of said load device (item 2) and which supplies an output of said semiconductor device to said load device (item 2); and a feedback interconnection which connects the feedback terminal (item 4) with the input terminal of said load device or said output interconnection and which feeds back a voltage supplied to said load device, to said semiconductor device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Rutland-Wallis whose telephone number is 571-272-5921. The examiner can normally be reached on Monday-Thursday 7:30AM-6:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MRW

BRIAN SIRCUS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800